REMARKS/ARGUMENTS

Reconsideration of the Application in view of the above amendments and the following remarks is respectfully requested.

The Examiner rejects claims 11 and 22 under 35 U.S.C. 103(a) as being unpatentable over Cha et al. in view of Mical et al. and Sasaki et al. The Examiner states that as to Claim 11, Cha et al. teaches a module for a display device comprising a wiring substrate having a single level of wiring and specifically refers to Item 62 in FIGURE 3 and Item 92 in FIGURE 5, and in the description at Col. 5, Lines 27-31 and from Col. 5, Line 66 to Col. 6, Line 1. The Examiner states that Cha et al. does not teach that wiring connected to the end input terminals to coupled data signals are parallel lines and states that Sasaki et al. teaches wiring connected to the end input signals to coupled data signals being parallel lines. The Examiner states that Mical et al. teaches a cross-over unit which can place appropriate even or odd-numbered pixel signals on respective side buses. The Examiner concludes it would have been obvious to one of ordinary skill in the art at a time of the invention to combined Sasaki et al. and Mical et al. with Cha et al.

This rejection is respectfully traversed. First of all, the Examiner chose to ignore the arguments in our previous response that Cha et al. does not show the wiring at all and thus, the Examiner's statements that the wiring is a single level of wiring, is unsupported. Although, the Examiner has not so stated, it seems that the Examiner is utilizing FIGURE 6 as the basis for this. However, it is clear from the drawing in FIGURE 5, that it is physically impossible to utilize a single level of wiring with the Cha et al. device. I order to explain this clearly, we also refer to FIGURE 7 of the present

application. In Cha et al.'s FIGURE 5, the wiring 84 must deliver the same bits to all of the devices 40 connecting the portion 80 with the display 10. Looking at FIGURE 7 of the present application, a similar structure is shown in this view of the prior art. As can be seen from FIGURE 7, and as well understood by those skilled in the art, there is no way to physically bring the lines D0 – DN up to each of the drive circuits 20 without making a 90-degree turn in the wiring at each device, it is well understood to those skilled in the art that such a turn can not be made between parallel lines utilizing a single level of wiring. This is clearly depicted in FIGURE 7 of the present application.

Similarly, the wiring 94 which comes up to the portion 92 must turn both to the left and right directions and then turn again towards the top of the drawing and these turns can not be accomplished utilizing a single level of wiring where the wires 94 are in parallel.

It is for this reason, that the present invention was needed in order to avoid the utilization of the two or more layers of wiring that will be needed. The fact that the number of layers of wiring is omitted from Cha et al., does not change the physical fact that it is simply impossible to have the parallel conductors change direction and be coupled to all of the devices utilizing a single level wiring. Claim 11 already recites a plurality of integrated circuits mounted on the wiring substrate if the wiring substrate has a single level of wiring thereon. It also recites that the inputs of the devices are arranged linearly in a row along the first side. However, in order to clarify the claim further, Applicant has amended Claim 11 to recite that the single level of wiring on the wiring substrate is connected to the end input terminals to couple data signals to the inputs of the switching circuits. Applicants respectfully submit that without the present invention, the coupling of the signals to the inputs of the circuits 42, 52, in FIGURE 5 of Cha et al. can not be accomplished without multi-level wiring.

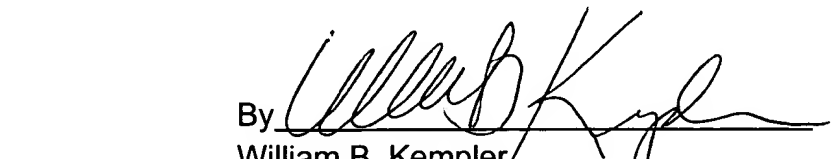
The Examiner states that Mical et al. is analogous art because the reference is reasonably pertinent to the particular problems which the Applicant was concerned. This statement is respectfully traversed. Mical relates to mutli-line video signal interpolation. In Mical et al., as stated by the Examiner in the present action, the cross-over unit places an appropriate even or odd–numbered pixel signals on respect of side buses. In sharp contrast, in the present invention, the input terminals are either coupled to the output terminals in increasing or in a decreasing order, that is, the order which the signals are coupled is reversed from one integrated circuit to another. This is not shown or suggested by Mical et al. Accordingly, combining Cha et al. with Mical et al. does not render the present invention obvious.

The Examiner has allowed claims 14 – 19 and 21. All of the remaining claims are dependent directly or indirectly from Claim 11. The patentability of Claim 11 having been shown above, these claims are patentable for the same reasons.

According, Applicants believe the Application, as amended, is in condition for allowance, and such action is respectfully requested.

Respectfully submitted,

Texas Instruments Incorporated

By 

William B. Kempler
Senior Corporate Patent Counsel
Reg. No. 28,228
(972) 917-5452